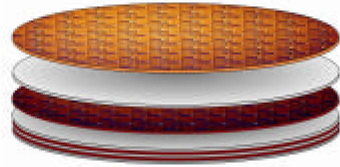
WholeWaferDeconstruct (WWD) Application Notes



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1. CMP for Yield Enhancement and Failure Mode Analysis

The ability to create planar surfaces during wafer construction has made Chemical Mechanical Planarization (CMP) one of the key enabling technologies in the development of ever-smaller IC chip geometries and ever increasing number of layers of interconnect.

The same CMP technology used to create a planar surface during wafer "construction" can also be used to maintain a planar surface during wafer "deconstruction". This is the principle behind Strasbaugh's Whole Wafer Deconstruct (WWD) process.

One of the main attributes of using a high quality CMP tool for WWD is the repeatability of the process. Once a process is developed to polish material down to the target layer on a particular wafer, the process can be stored as a menu in the system memory and recovered as required.

Another attribute of using a high quality CMP tool for WWD is flexibility, which allows for rapid process optimization on a variety of oxide and metal films, on many different product wafers.

2. A CMP Tool for the FMA Laboratory

Modern semiconductor CMP has its origins in precision optics manufacturing. Precision optics tools themselves however, did not have the repeatability, stability or automated process control necessary for semiconductor manufacturing. The widespread implementation of CMP had to await the development of special semiconductor quality planarizers.

Strasbaugh's Model 6EC and 6EG planarizers bring this technology out of the Fab, and make it available to Yield Enhancement and FMA Engineers in a laboratory.

Strasbaugh's laboratory CMP tools pack all of the process capability of full-scale CMP tools into a much smaller footprint at a fraction of the cost. The space and cost savings are achieved by the elimination of the components needed for automated wafer handling.

Deconstruct via whole wafer CMP can serve to complement or completely eliminate the chemical etching process. When etching through six or more layers of metal, a number of different chemicals may need to be utilized, resulting in a process that could take days.

WWD provides the most comprehensive picture a FA engineer can have to rapidly and accurately identify design or manufacturing yield issues.

3. The WWD CMP Process

The CMP process used in WWD is similar to CMP used in wafer manufacturing. There are, however, key differences, and understanding them will give an insight into the characteristics of the process.

The principle differences can be stated as follows:

CMP used in Semiconductor Manufacturing:

- Each layer on the wafer has its own specific CMP process.
- Slurries are used that have a high selectivity for one material only.
- The process is optimized to give high removal rates on the layer being polished.
- The goal is to planarize the topography on the wafer to produce the flattest surface possible with the highest wafer throughput.

CMP used for WholeWaferDeconstruct (WWD):

- In WWD, the same CMP process is applied to ALL of the layers on a wafer.
- Slurry selectivity is “biased” to give lower rather than higher removal rates in the target layer.
- The goal in WWD is not to produce the flattest surface possible, but rather to duplicate the uniformity and flatness of the original layers on the wafer.
- The goal in WWD is generally to produce an intact target layer on the wafer surface that will be receptive to a variety of failure analysis (FA) techniques.

4. A Single CMP Process for all of the Layers on a Wafer

The CMP processes used in manufacturing are optimized for each single layer, with several different processes and consumable sets used to planarize the different layers on a product wafer. This, however, is not an effective strategy for WWD.

The time taken to swap consumables and change the process parameters several times during WWD on a single wafer would more than offset any removal rate, or uniformity advantage, in using a separate process optimized for each layer.

WWD processes are generally designed to stop within a given layer such as an ILD or IMD. Unlike IC wafer manufactures, we rarely stop a WWD process at a boundary between two layers on a wafer, and as such, very high process selectivity is not required to prevent erosion and dishing of the underlying layer.

Very high selectivity is not required for WWD, but we do adjust the process selectivity to slow the process during polish of the target layer. Lowering removal rates in the target layers widens the window of time in which we can stop the process, and still retain the desired thickness of target layer material.

5. Consumables Employed for Strasbaugh WWD CMP Solutions

The ability to use one process to deconstruct a whole wafer greatly enhances the utility of the process. Not only can within-die wafer failures be quickly identified, but across-the-wafer failures can also be quickly revealed (e.g., die in center of wafer analyzed against the die on the edge of the wafer).

Carrier Film	Strasbaugh pre punched DF200 psa 2,
Primary Table Polish Pad	Blown Urethane
Slurry Type One: Intra-layer TEOS (P) Top Passivation Layer (P)	Oxide Slurry A DI Water
Slurry Type One: Al/TEOS (P) W (B) TEOS (B)	Metal Slurry A DI Water
Slurry Type One: Cu/TEOS (P) Cu (B) TEOS (B)	Metal Slurry B DI Water
(B= Blanket wafer, P= pattern wafer)	

5.1 Metal Slurry A: Al/TEOS WWD Slurry

Illustrates the differences in Metal A slurry mixtures.

Ratio	Oxidizer	DI Water	Abrasive	Rate Adjuster	Comments
Metal Slurry-A1	2	4	2	1	Strong metal slurry
Metal Slurry-A2	1	2	1	1	Weak metal slurry

** A higher quantity of oxide adjuster in the slurry mixture makes the Metal slurry more efficient at removing an oxide film.*

Removal Rate comparison

	Removal Rate (Ang./minute)		
	Oxide Slurry A	Metal slurry-A1	Metal slurry-A2
Thermal Oxide	2100	618	900
Tungsten or Aluminum	N/A	3000	1800
Removal Ratio (Al:THOX)	N/A	5.0:1	2.0:1

Strasbaugh THOX wafers were used to improve the global uniformity.

5.2 Metal Slurry B: Cu/TEOS WWD Slurry

Illustrates the differences in Metal A slurry mixtures.

Ratio	Oxidizer	DI Water	Abrasive	Comments
Metal Slurry - B1	2	1	1	Standard (1:1:1)
Metal Slurry - B2	2.5	1	1.5	Strong metal slurry
Metal Slurry - B3	1.5	1	0.75	Weak metal slurry
Metal Slurry - B4	1.5	1	1.5	High TEOS

** A greater quantity of abrasive in the slurry mixture makes the Metal slurry B more of an oxide slurry: more efficient in removing oxide film.*

Removal Rate comparison.

Removal Rate (Ang./minute)	Oxide Slurry A	Metal slurry-B1	Metal slurry-B2	Metal slurry-B3	Metal slurry-B4
Thermal Oxide	2100	1000	NA	NA	NA
Copper	N/A	1000	NA	NA	NA
Removal Ratio (Al:THOX)	N/A	1:1	NA	NA	NA

Strasbaugh THOX wafers were used to improve the global uniformity.

6. Consumable Applications

6.1 Oxide Slurry A

6.1.1 Passivation Layer Removal

WWD processing normally begins at the passivation cap above the top metal layer on a wafer. *It is very important that any polyimide film layers or "bumps" are removed above the passivation layer prior to WWD process.*

Strasbaugh employs oxide slurry A for several operations during WWD; one is to remove the passivation layer (silicon nitride + oxide) to expose the top metal layer on an IC wafer. We have observed this slurry to yield an optimum combination of process WIWNU and Removal Rate.

Carrier Film	Strasbaugh pre punched DF200 psa 2,
Primary Table Polish Pad	Blown Urethane
Slurry Type: Intra-layer TEOS (P) Top Passivation Layer (P) Machine Baseline Testing (B)	Oxide Slurry A DI Water
(B= Blanket wafer, P= pattern wafer)	

Optimal process results using blanket oxide wafers evaluated at a 6mm Edge Excl.

Wafer Type	Slurry Employed	Removal Range (A)	Removal WIWNU (%)	Removal (um)	Removal Rate (A/min)	BENU (%)
Thermal Oxide	Oxide Slurry A	920	3.3	5558	2030	-0.3
TEOS Oxide	Oxide Slurry A	921	2.6	8898	3559	1.8

- Wafers evaluated using a 49pt polar map at a 6mm edge exclusion

6.1.2 Intra Layer ILD/IMD Planarizing

A secondary application for WWD is to planarize an ILD layer following a previous dry or wet-etch process. This application requires the flexibility, precision and planarization capability of a high quality CMP tool. Topography, which is created by the etch process, must be removed on the surface at the target layer prior to performing FA testing. Strasbaugh employs oxide slurry "A" for this "high planarization efficiency" application.

Average step height Planarity results for Intra layer TEOS oxide polishing

Wafer ID	Slurry Employed	Process Requirements	Polish Time (min)	Average of Sites 1-9 PRE/POST (Ang)	Planarization Efficiency (%)
1	Oxide Slurry A	ILD Planarization Removal Target = 4000A	1.0 min	6000/836	86
2	Oxide Slurry A	ILD Planarization Removal Target = 4000A	1.0 min	6000/889	85
3	Oxide Slurry A	ILD Planarization Removal Target = 4000A	1.0 min	6000/786	87
4	Oxide Slurry A	ILD Planarization Removal Target = 6200A	1.5 min	6000/444	93
5	Oxide Slurry A	ILD Planarization Removal Target = 6200A	1.5 min	6000/354	94
6	Oxide Slurry A	ILD Planarization Removal Target = 6200A	1.5 min	6000/412	93

* Scan length = 3500um

6.1.3 Model 6EC & 6EG Planarizer Qualification

Strasbaugh currently recommends the use of oxide slurry A as part of the consumables set employed to establish baseline tool performance.

6.2 Metal Slurry A

6.2.1 Multi Layer Planarizing of AL/TEOS IC wafers

Strasbaugh employs the Metal Slurry A to perform its conventional WWD process on Al/TEOS wafers. Metal slurry A provides the flexibility and repeatability to accurately target either a metal or oxide layer within the multi-level metal interconnect.

Carrier Film	DF200 psa 2, pre punched
Primary Table Polish Pad	IC1000 xyk-grv/Suba IV, Rodel
Slurry Type One: Al/TEOS (P) W/TEOS (P) W (B) TEOS (B)	Metal Slurry A DI Water

Optimal process results using blanket oxide wafers evaluated at a 6mm Edge Excl.

Wafer Type	Slurry Employed	Removal Range (A)	Removal WIWNU (%)	Removal (um)	Removal Rate (A/min)	BENU (%)
Thermal Oxide	Metal Slurry A	130	0.8	3557	593	-0.1
TEOS Oxide	Metal Slurry A	155	1.0	4462	744	-0.7

- Wafers evaluated using a 49pt polar map at a 6mm edge exclusion

6.3 Metal Slurry B

6.3.1 Multi Layer Planarizing of Cu/TEOS IC wafers

Strasbaugh employs the Metal Slurry B to perform its conventional WWD process on Cu/TEOS wafers. Metal slurry B provides the flexibility and repeatability to accurately target either a metal or oxide layer within the multi-level metal interconnect.

Carrier Film	DF200 psa 2, pre punched
Primary Table Polish Pad	IC1000 xyk-grv/Suba IV, Rodel
Slurry Type One: Al/TEOS (P) W/TEOS (P) W (B) TEOS (B)	Metal Slurry A DI Water

Optimal process results using blanket oxide wafers evaluated at a 6mm Edge Excl.

Wafer Type	Slurry Employed	Removal Range (A)	Removal WIWNU (%)	Removal (um)	Removal Rate (A/min)	BENU (%)
Thermal Oxide	Metal Slurry B	NA	NA	NA	NA	NA
TEOS Oxide	Metal Slurry B	NA	NA	NA	NA	NA

- Wafers evaluated using a 49pt polar map at a 6mm edge exclusion

7. Stopping the Process in the Target Layer

After process characterization, a realistic goal for WWD on a Model 6EC or 6EG for most wafers is to be able to automatically polish the wafer and stop the process in a +/-1500 Angstrom ILD target window directly from a stored polish recipe.

The two principle factors, which make this possible, are:

- The high degree of stability, repeatability and control provided by a state-of-the-art CMP tool. The Strasbaugh Model 6EC and 6EG CMP tools incorporate closed loop control of all operating parameters
- A highly repeatable process designed to lower removal rates in the target material.

Successful WWD process removing 5 layers of interconnect, and 100kA of material to a targeted ILD-l

WholeWaferDeconstruct Demonstration at Strasbaugh:

Oxide on top of Metal 1

	NOTCH	CENTER	TOP	LEFT	RIGHT	Std Dev.	Avg Thickness Removal (A)	WIWNU % (1 sig)	Post Range (A)	
Wafer 1	2740	2625	4920	3070	2935	945	3258	29.0	2295	
Wafer 2	3290	3435	4245	3280	2540	607	3358	18.1	1685	

Material Removed

	NOTCH	CENTER	TOP	LEFT	RIGHT	Std Dev.	Avg Thickness Removal (A)	WIWNU % (1 sig)	Polish Time (min)	Removal Rate (A/min)
Wafer 1	98110	98225	95930	97780	97915	945	97592	0.97	59	1654
Wafer 2	97560	97415	96605	97570	98310	607	97492	0.62	55	1773

Total Thickness ILD 1 through ILD 6. (A)= 100850

- Process optimization or final iterative polishing could further improve these values.

8. Post Process Planarity (BENU)

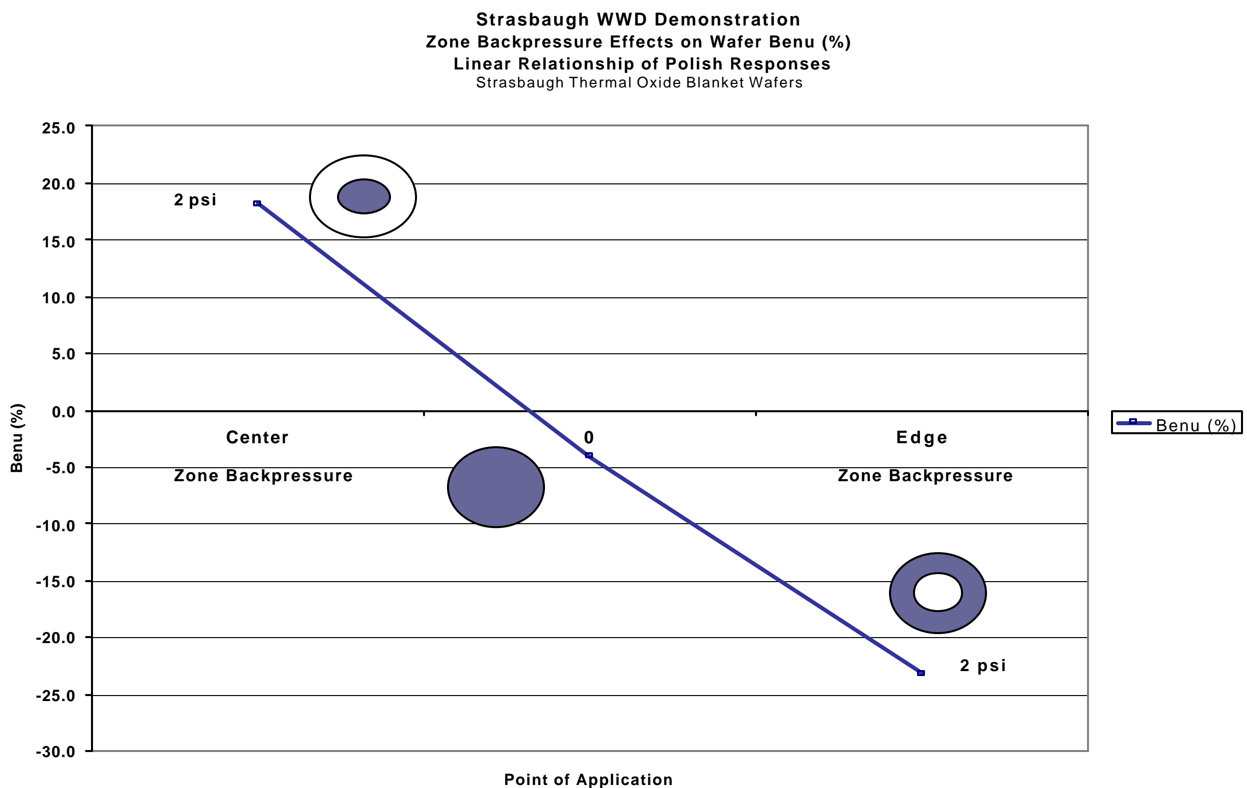
When CMP is used in the construction of a wafer, the aim is to produce a surface, which is as planar or flat as possible. Modern CMP tools are very good at this, but even so, a degree of non-uniformity can still creep into the process during manufacture. This usually takes the form of Bulls Eye Non-Uniformity, where there is a center to edge variation in film thickness.

In WWD, we do not aim solely for the optimum planarity or flatness. Instead, our primary goal is to sustain the same uniformity that was created when the wafer was manufactured. If the original layers on a wafer exhibit positive BENU (concave surface), the WWD process must also exhibit a positive BENU in order to be able to stop the process in the middle of the target layer, and leave a uniform layer of target material intact.

For this reason, conventional measurements of planarity do not have much meaning in WWD. We expect to be able to stop the process within a +/- 1500 Angstrom window which equates to 3-5% within wafer non-uniformity.

9. Zone Backpressure

BENU is controlled on Strasbaugh Model 6EC and 6EG planarizers by the use of Zone Backpressure in the wafer carrier. This feature allows the user to dial in any required degree of positive or negative BNU to match the planarity of the target layer.



10. Material Removal Rates and Process Times

Because of the different film materials, pattern densities, and layer thicknesses that must be polished in a WWD process, it is not possible to give a truly accurate figure for removal rate for a specific application. Generally to date most WWD processes polish near a rate of 1-1.5kA/min.

Therefore, as a rough guide, it should be possible to polish through a 6 metal Al/TEOS wafer and stop the process in ILD-1 in approximately one hour. Approximately ten minutes per ILD.

Approximate polish times and film tacks for a 6 level multi level interconnect IC wafer.

Layer	Al/TEOS	Thickness (A)	Approx. Polish Time/Layer (Total Time)	Cu/TEOS	Thickness (A)	Approx. Polish Time/Layer (Total Time)
Passivation	Nitride / Teos	12000	6 min	Nitride / Teos	12000	6 min
M6	Al / Ti	12000	10 min (18min)	Cu	12000	10 min (18min)
ILD5	Teos or HDP	7500	6 min (23min)	TEOS	7000	6 min (23min)
M5	Ti-Nit / Al / Ti-Nit / Ti	9000	6 min (29min)	Cu	5500	6 min (29min)
ILD4	Teos / HDP	7500	6 min (35min)	TEOS	7000	6 min (35min)
M4	Ti-Nit / Al / Ti-Nit / Ti	9000	6 min (41min)	Cu	5500	6 min (41min)
ILD3	Teos / HDP	7500	6 min (47min)	TEOS	7000	6 min (47min)
M3	Ti-Nit / Al / Ti-Nit / Ti	6000	6 min (53min)	Cu	5500	6 min (53min)
ILD2	Teos / HDP	7500	6 min (59min)	TEOS	7000	6 min (59min)
M2	Ti-Nit / Al / Ti-Nit / Ti	6000	6 min (65min)	Cu	4500	6 min (65min)
ILD1	Teos / HDP	7500	Stop	TEOS	7000	Stop
M1	Ti-Nit / Al / Ti-Nit / Ti	6000		Cu	4500	
	Teos	4500		W	600	
	Teos	5200			8000	

11. Surface Finish after WWD CMP

The surface finish produced after WWD CMP is of commercial Optical Quality, and requires no additional polishing for inspection.

12. Process Development

To develop a process capable of being stopped at any specified ILD layer on a wafer would typically be done as follows;.

1. Polish 5-10 blanket oxide wafers deposited with the same ILD material that is used on the product wafers. Oxide represents the bulk of the material on a product wafer, and this baseline oxide removal rate data is helpful in developing the process for more expensive product wafers.

2. Polish a product wafer down to the target, layer by layer to record process times. At that time we also make adjustments to the process to improve the final uniformity of the target layer on subsequent wafers.

3. Repeat the process on the product wafers until 1 polish step is required to target and stop the process within a thickness range on a specific layer.

A supply of 10-blanket oxide and 10 product wafers are usually sufficient to allow a good process to be developed for a specific target layer on a wafer with six layers of metal interconnect. The process can then be "tuned" to adjust to other target layers in an efficient manner.

13. Process Demonstrations by Strasbaugh

Strasbaugh is happy to perform initial feasibility demonstrations of WWD, stopping the process on one or two target layers in a wafer. In addition to showing the capability of the tools, the demonstrations also serve to establish an initial baseline for the customers' own WWD process and specified target layer(s).

To perform a WWD Demonstration, we require the following materials from the customer.

1. 10 Blanket oxide wafers deposited with the same oxide used in the product wafer ILD.

2. 10 Product wafers.

3. Clear plan-view photographs of each metal layer in two magnifications, (i.e. 10X and 50X magnification) to allow Strasbaugh's process engineers to identify the different layers on the wafer.

4. A sketch of the vertical structure of the wafer, showing the thickness and material of the layers that will be encountered.

5. Measurement sites for post polish ILD thickness evaluation.