Multiple Failure Analysis Applications Using Strasbaugh nOvation System

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Abstract

The focus of this paper is on failure analysis using the Strasbaugh nOvation grind/polish tool to quickly prepare whole wafer for thermal FA and PFA techniques inspections, especially for whole wafer super thinning (WWST) and whole wafer deconstruction (WWD).

Introduction

Failure analysis (FA) is a critical element during all phases of the integrated circuit (IC) manufacture. The goal of FA is to determine the root cause of a failure or parameter excursion so that corrective action can be taken for yield enhancement.

There are a plethora of techniques available to the FA community. In general the techniques can be grouped into categories such as electrical test and measurement, optical and scanning laser microscopy, physical failure analysis (PFA) such as wet/dry etching or whole wafer deconstruction (WWD) for layer removal, and thermal analysis such as using infrared technology, electron beam, photon emission, ion beam and scanning probe such as AFM, STM etc. [1-3].

For Infrared (IR) analysis, which includes photoemission analysis (imaging of devices and the 1st metallization layer) and thermal emission (imaging of hot spots) through the substrate backside, the backside of the wafer must be thinned and polished to a mirror finish.

Each of the FA methods has its advantage. The most of advanced inspection techniques require a great amount of the time for sample (wafer) preparation. Sometimes the processes of dicing, grinding and etching dies/wafers can require several days or even weeks. These techniques are often manual processes that require a highly skilled technician and the quality of the end-result is often unpredictable and unacceptable.

This paper focuses on a fast (less then 2 hours) whole-wafer inspection preparation for thermal FA and PFA techniques, using the Strasbaugh nOvation grind/polish tool for both whole wafer super thinning (WWST) and whole wafer deconstruction (WWD).

WWST for Thermal FA

One of the processes that the Strasbaugh nOvation system is designed for is the preparation of wafers for thermal failure analysis within a short time frame (20min to a few hours) by whole wafer super thinning (WWST). This advanced method provides the FA community with a revolutionary means of device access through the backside of the silicon wafer. By thinning the wafers to 100 – 300um thick (removing ~ 60% – 85% of the Si) and then polishing the ground surface, clear images of the devices built into the surface of the Si wafer can be

obtained through the backside of the wafer. By leaving the front side of the wafer intact the devices can be probed and energized (activated). An IR microscope can detect any hot spots on the device that indicates excess heat is being generated and not efficiently being carried away. These two images can then be overlaid and the location of the hot spots (defects) can be identified.

For WWST the nOvation tool is both a grinder and a polisher with the wafer held securely face up on a vacuum wafer chuck. Grinding wheels and or polishing pucks are held in an over arm by vacuum and can be quickly swapped. Process force is applied by the lower wafer chuck moving up to contact and press against the upper spindle mounted in the over arm. During process the force is held constant and as material is removed from the wafer and the wafer chuck moves up only to keep the force constant. This force control is needed in order for the tool to polish wafers with either fixed abrasives or standard CMP consumables.

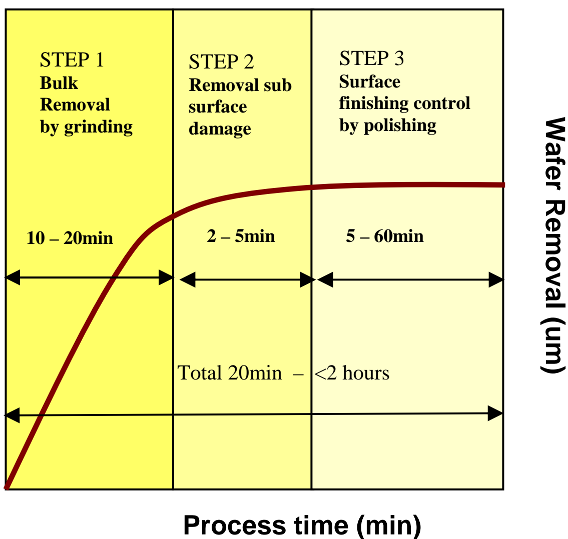

Figure 1. WWST grinding and polishing process

Figure 1 shows the 3-step process of WWST. Step 1 endpoints on removal to meet the bulk substrate removal target. With process optimization, the accuracy of the targeted wafer removal can be lower then the 20µm specification. Figure 2 displays a wafer run where the removal was less then 3µm from the target.

Step 2 of WWST is removing sub-surface damage by fine grinding. The last step is controlling surface finishing by polishing. During the process, non-contact in-situ measurements of the wafer thickness are tracked by software and used to endpoint. Table 1 lists the WWST results.

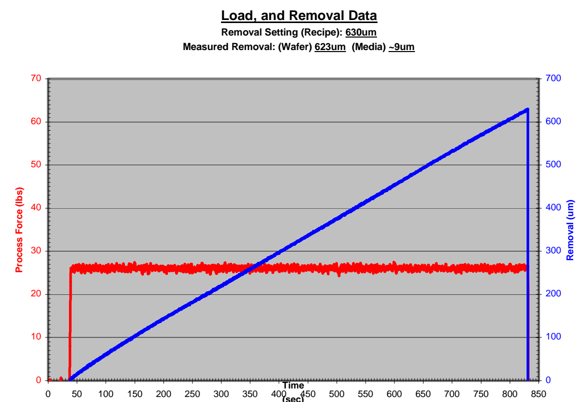

Figure 2. WWST step 1 removal process

Table 1.nOvation WWST Results

	Wf Input	WWST wafer final results		
		Spec	Results	
			200mm	300mm
ThK, um	780 - 820	<200	80	100
Rate um/min		>25	60 - 120	30 - 60
TTV, um		<20	6-Apr	<10
Scratch		None	None	None
Surface Finishing		Mirro finish	Mirro finish	Mirro finish

WWD for PFA

Physical failure analysis, on the contrary, is often required to delayer samples from the device side until failure defects are visible.

Single die wet/dry etching techniques (i.e. RIE) are still used in the industry. However, they are considered to be an extremely time consuming, i.e. 1 to 7 days. Whole wafer deconstruction technique can increase the efficiency in PFA tremendously. It usually takes less then 2 hours to prepare a whole wafer of samples.

Typically the delayering process is stopped in a via (dielectric) layer above the metal layer of interest so not to expose the defect but allow it to be inspected using optical or other techniques.

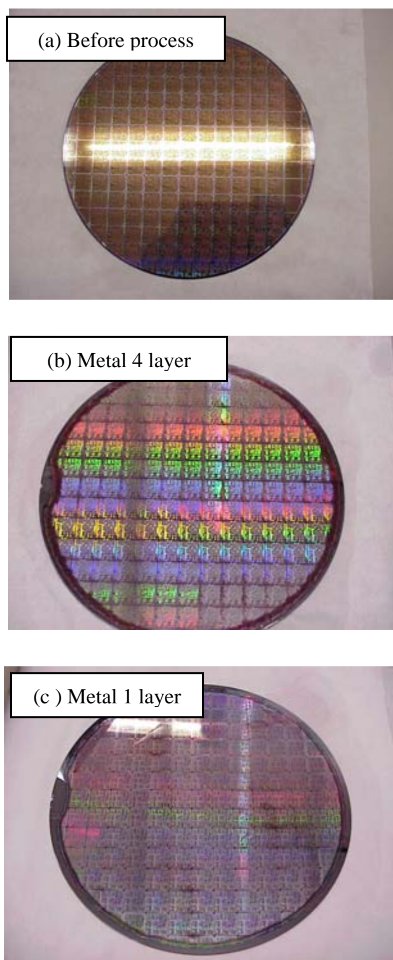

Figure 3. Whole wafer deconstruction by nOvation.

For the WWD wafer handling, the standard vacuum chuck can be quickly fitted with wafer backing inserts and retaining rings to allow the wafer to be secured device-side up. Sub-aperture (i.e., sub-diameter) design uses polishing elements smaller in diameter than the wafer itself. The operator can see the delayer process and make adjustment as needed. Figure 3 shows the results at various stages in the WWD process. It can be seen that by delaying the wafer from Metal 4 down to Metal 1, the wafer is processed uniformly with minimized edge exclusion. Figure 4 is a site top view of a defect exposed by WWD.

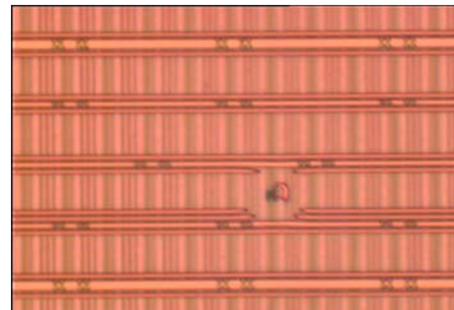

Figure 4: Site top view of a defect after polishing down and stopping within the via layer above, but not exposing the defect.

Conclusion

Failure analysis (FA) is a critical element during all phases of the IC manufacture. Thermal FA requires a super thin wafer to analysis the defects on device side through the backside. The physical failure analysis is often required to delayer wafers from the device side until failure defects are visible. Both methods usually require long (up to a week) preparation times for individual dies.

Using nOvation system both whole wafer super thinning (WWST) and whole wafer deconstruction (WWD) preparation times of

whole wafers are shorten from days to less then 2 hours.

The WWST process results achieved 60-120um/min and 30-60um/min removal rates for 200mm and 300mm wafer size, respectively. The WWD process can be done with wafer face up that operator could see the delaying process. The system allows wafers as large as 300 mm. to be processed in a compact machine that takes up minimal floor space (~8ft^2).

References

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