Using CMP-Process in PFA for whole Copper Wafers Deconstruction

Christian Hobert[1], Lily Yao[2], Bryan Sennett[2]
[1]AMD Saxony Limited Liability Company & Co. KG, D-01109 Dresden, Germany
[2]Strasbaugh, 825 Buckley Road, San Luis Obispo, CA 93401
christian.hobert@amd.com Lily_Yao@strasbaugh.com

Abstract

A key method for yield learning is physical failure analysis. Defects and structures of interest are often buried beneath a multi level metalization stack.

Here deconstruction processes come into play capable to remove layers in a controlled manner. Copper metalization production processes, when introduced, brought new challenges to the PFA-community, which needed to be solved.

Whole-wafer-deconstruction processes have been implemented for quite some time in aluminum backends, but copper wafers were still broken into pieces for deconstruction and analysis. This article will highlight the general differences between aluminium and copper backends, the development of a CMP-based deconstruction process for fully processed copper wafers, further steps in improving and automating this new process and its benefits for the daily PFA work.

Introduction

Physical Failure Analysis (PFA) is used as an analysis method helping semiconductor-manufacturing sites shorting yield learning cycles.

By the end of the last century the semiconductor industry lead by IBM, Motorola and AMD introduced new production processes based on copper interconnects. Compared with the well-known delayering methods developed for wafers and dies with an aluminum backend it was now also a perfect time to develop new strategies and methods helping the PFA community to work as efficient as possible with this new metalization stack.

In PFA it is often required to delayer samples in a controlled way to expose regions of interest or explore failed sites. Many PFA-teams are still working on single dies to find the nature of a failing site. Production environments have different or additional needs:

- the response time needs to be fast to reveal Fab issues quickly, so the sample preparation time should be very short,
- wafers are rather costy, so the most information one can get out of it to draw conclusions to improve the fab process is a must.

Deprocessing entire wafers can increase the efficiency in PFA tremendously, so the number of samples prepared at once and hence the possibility to explore much more sites in an wafer inspection tool in one step is very beneficial.

This potential can be also used in the development phase of new technology nodes such as 90nm and 65nm, where the Fab engineers need sufficient input about their process development.

Several deconstruction options were evaluated. Polishing (or grinding) was one of the options looked at and considered to be the most favorable way of providing a thorough method of controlled delayering.

What are the differences between the aluminum and copper deconstruction methods?

The aluminum backend:

Due to the fact that most aluminum backends consist of two different conductive chemical components (aluminium (metal lines) and tungsten (contacts)) one is able to remove one layer very selectively at a time by using a combination of wet and/or dry (RIE) etch steps.

Depending on the methodology used this might take about 1.5-2.5 hours of preparation time for each of the metal stacks and interconnecting vias. So the total preparation time of a wafer or a die can take up a one day before one reaches the layer of interest.

The Copper Backend

The Copper Backend brought new challenges into the life of the PFA-community. There is a new chemical component Copper. As shown in Figure 1 metal trenches and vias are filled with copper(dual damascene). The selective controlled removal of just the metal trench or just the via using wet etch chemistry, as known from the aluminum process, is very difficult and one loses planarity control rapidly.

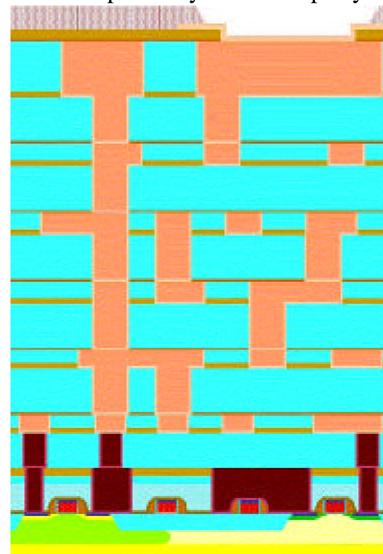

Figure 1. Schematic Cross Section through a Copper Backend

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The development of a polishing process optimized for Copper Wafer deconstruction

A thorough market survey for wafer polishers was performed looking for a tool able to meet the needs in daily operations in a lab environment. This tool should be easy to operate, flexible enough to adjust the process parameters, have a small foot print and low operation costs. Last but not least there are certain process conditions, which need to be fulfilled as well. Those cover the abrasion rate (polish time), uniformity and repeatability.

The conducted survey actually returned only one supplier offering a polisher for Lab-Application, Strasbaugh's 6EC – a 200mm wafer polisher intended for Fab-Process development.

In late 1998 the AMD-Fab30 Product Engineering Team began with the evaluation of the 6EC for whole wafer deconstruction.

First experiments were performed on aluminum backend wafers, which faced the process engineers at Strasbaugh with new challenges. After several process iterations they came up with an just recipe using an abrasive slurry, which removed the top site passivation, two complete metal layers and stopped in an ILD without exposing the under-laying metal layer within one hour, relatively good across wafer and within-die uniformity.

In a second step the "aluminum process" was applied to six-metal-layers copper backend wafers. The first Cu/TEOS wafer was very difficult to polish compared to the aluminium wafers. The removal rate was very low in particular in the wafer center area. Thus the process needed to be tweaked. Here helped the special feature of the wafer to apply zone dependent backpressure to the wafer.

Still the polish times were still not in an acceptable range (up to 210 minutes for the removal of three metal layers). In afford to reduce the polish time a higher polish pressure and higher table speeds were applied in the process but the polish pads wore out very fast and had to be exchanged after each wafer. This initial copper approach did not meet the criteria set as a goal.

So the "just abrasive" methodology had to be thought over.

The final process

The solution could only be a Chemical Mechanical Polish (CMP) Process. The Strasbaugh engineers in cooperation with EKC Inc. developed a slurry mix based on a Copper Oxidizer and Metal CMP Polishing Slurry (Slurry A).

The new process is a multiple step process, which uses in-situ pad conditioning, different process pressure and table/spindle speed setting regimes for the different metal layers. The entire process used so far is time controlled.

Depending on the pattern density (ratio of copper and insulator) in each of the layers the process conditions can vary and for different chip designs too. So here the user-friendly recipe GUI to adjust/write recipes comes into play.

Polish Process Flow Example

1st Step: higher polish process pressure to break through the top site passivation and remove the top metal layer, which is thicker compared to the layers beneath (polish time ~6 min.);

2nd Step: (main step) reduced polish process pressure and adjusted table/spindle speed to assure a uniform process (polish time for 3 metalization layers ~15 min.);

3rd…(x-1)th Steps (if required): adjusted recipes for other metalization layers with different pattern density;

Last Step: surface finishing (very short 10 sec.), low polish process pressure and high table speed.

Polish result

A tremendous reduction in polish time (down to about 20-30 minutes for three metal layers) and a much longer polish pad life time (>15 wafers), because of a reduction of the polish process pressures, have been observed for the new process.

The across wafer uniformity as one part of the acceptance criteria was determined by FIB cuts placed across the wafer and the polish process progress by checking certain layer marks visually on the wafers during processing.

Typical polished wafers show a uniform (<300nm variation) opened wafer center area as large as 16 cm in diameter. The outer wafer edge area is often covered with residuals from remaining layer(s) (Figure 2). Further recipe adjustments could definitely improve the uniformity, but removing the outer "ring" is very difficult because of the production process inherent variability at copper polish. Even though the current process does not expose the wafer edge in the same ratio as the wafer center, the benefits of this new deconstruction methodology are obvious.

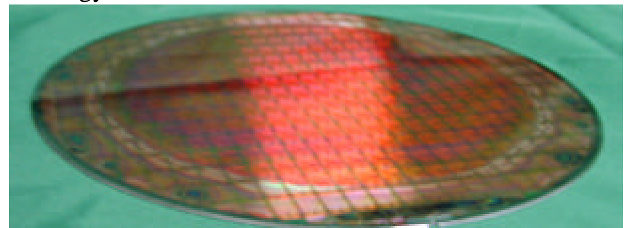

Figure 2. View on a polished Wafer

The average polish rate for the total process came out at about 200nm/min.

Because of manufacturing process variations the layer thicknesses and wafer uniformity due to i.e. CMP-reworks may vary too, the operator has to watch the polish progress really carefully to avoid any undesired overpolishing.

Deconstruction Example

Typical deprocessing is supposed to stop in a layer (i.e. via), so that the layer of interest below (i.e. metal lines) is still covered and not exposed.

Figures 3 shows an example of an embedded defect causing an interruption of metal lines exposed by polishing into the ILD layer above it and reviewed with a SEM.

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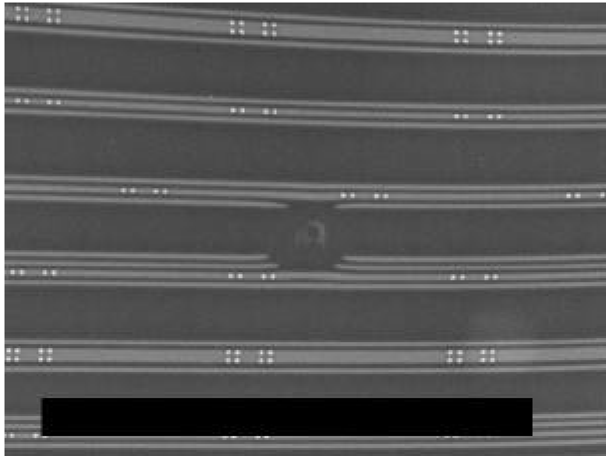

Figure 3. Failing site (SEM image)

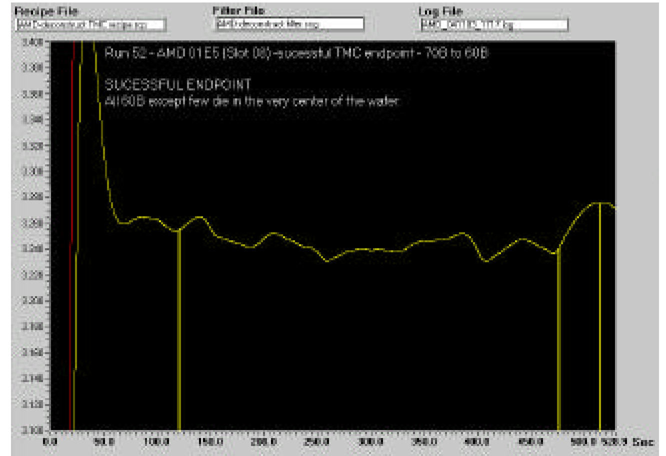

Figure 4. EPD for M6

Current Process Challenges

While copper backend wafer have increasing metalization layers (sometimes up to 9), delayering a wafer to a targeted layer becomes more of a challenge. The process has to be optimized layer-by-layer depending on the Metal/ILD density and pattern structures and even materials used.

In order to achieve significantly higher speed/device performance, copper must be integrated with low-k dielectrics; those films are softer than regular ILD and brought even more complication into PFA community. One type of slurry may not be enough. The slurry A used to deal with Cu/TEOS metalization up to 6 layers. The WWD (whole wafer deconstruction) process showed reasonable results with polishing rate, within die non-uniformity (WIDNU) and throughput. However while Cu/low-k stacks were introduced, using slurry A could only be successful for a few top layers that have Cu/Regular ILD structures (TEOS or FSG from M9 to M6, for instance). After low-k film are exposed, the process showed an aggressive rate on low-k film and slow rate on Cu. WIDNU became an issue also. Introduce slurry B with lower selectivity between Cu and low-k film is necessary. The process development is on going.

Process improvements

Since a while AMD and Strasbaugh are working closely on an polish endpoint detection (EPD) system implementation for the deconstruction process.

During the previous WWD development and field application, it requires engineers and technicians to watch the polishing process very closely and to take much longer time to develop a proper process. In order to control the process better, an EPD system (nPoint System with motor current) is introduced on Strasbaugh's 6EC polisher for WWD applications. Figure 4 shows one example of nPoint system output detecting the targeted metal layer (M6) successfully.

As mentioned above the difficulty of different chemical components used in the ILD stacks make it necessary to really comprehend the endpoint signals detected during the WWD process. The nPoint did not miss any endpoint signals while the process was approaching/reaching the metal layers.

Conclusions

Copper backend WWD using a CMP-based technique opened a new methodology in PFA. As a side effect a similar process can be applied to aluminium backend wafers as well based on the initial experiment.

The real gain for PFA is the tremendous time saving in sample preparation.

First the total wafer deconstruction, which took about one day or even longer, has been reduced to a few hours for a fully processed wafer (Bump removal, polishing, preparation for SEM/FIB). This enables PFA-teams to reduce the yield learning cycles effectively.

And second looking at the throughput gain: preparing a die takes almost as long as preparing now hundreds of dies on a wafer. In addition the efficiency of the 200mm wafer dual beam SEM/FIB system used for inspection has been increased as well.

Once the endpoint detection process has been fully characterized and the new polish process is stable it will improve the effectiveness of the tool even further.

For more than 3 years the WWD process has been successfully used in routine copper wafer deconstruction at AMD's Fab30 in Dresden.

Acknowledgments

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Reference

Christian Hobert, "Advanced Deconstruction Methodology for Copper Wafers", FUTURE FAB international, issue 13, July 2002, Section10, pp 281-283

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